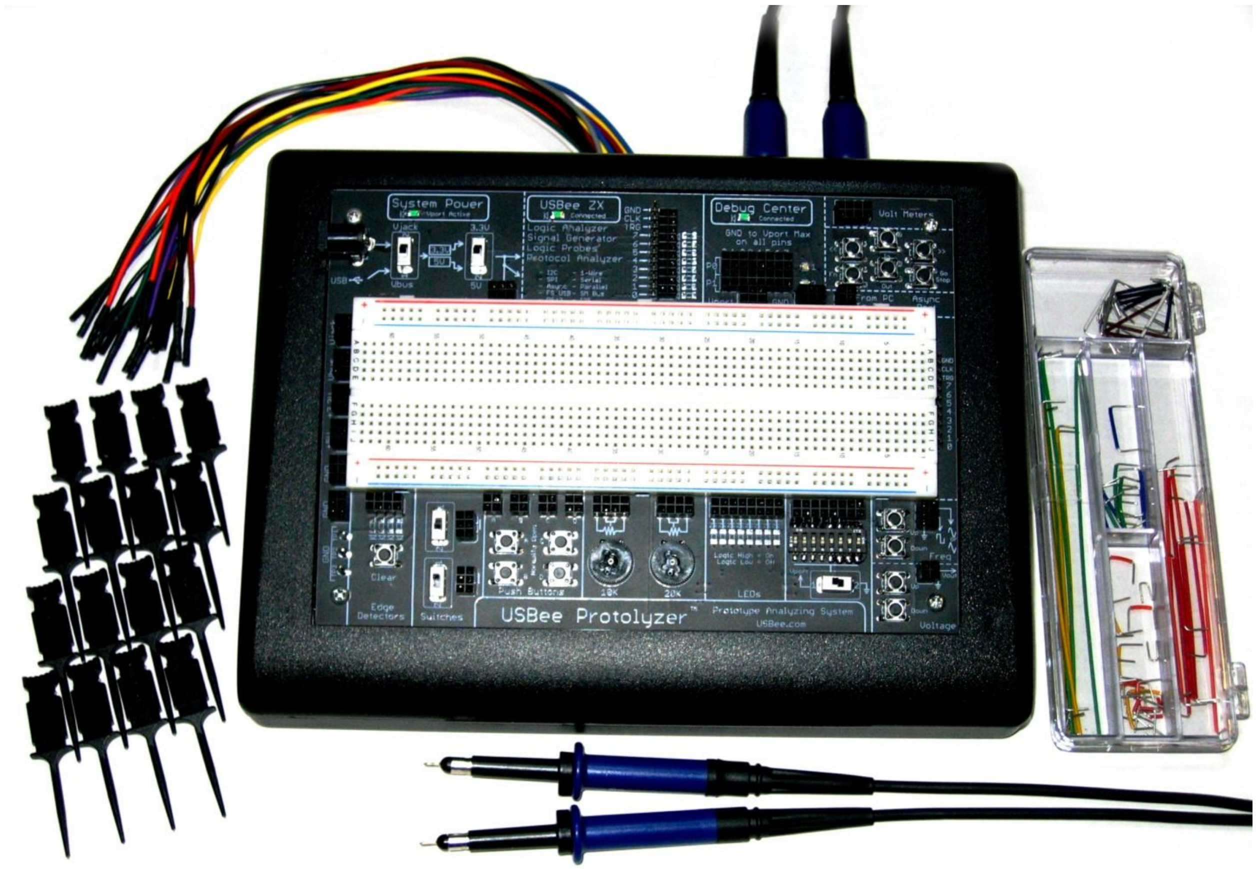
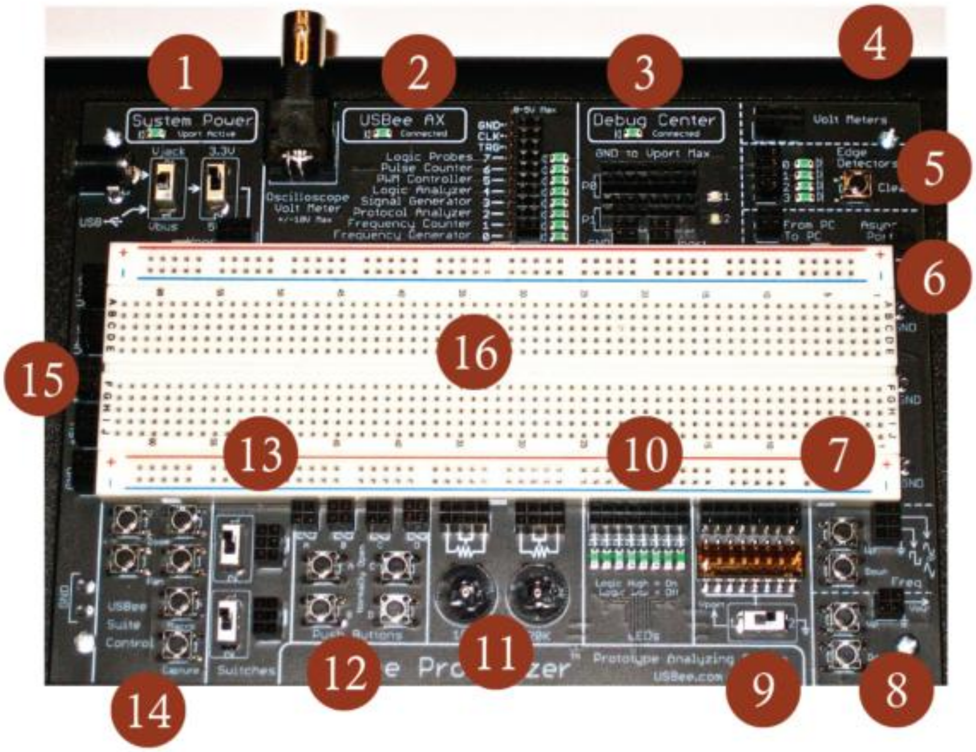


USBee Protolyzer Specifications

CWAV, Inc.

www.USBee.com

This document details the operational specifications of the USBee DX and AX Protolyzer. The photo below shows the top working surface of the Protolyzer. Included are reference numbers that are called out in the descriptions below.



Power (1)

System Power – Create the power supplies for your system here. Select either the USB VBus or an external 6V to 15V DC supply (sold separately, + center, -outside). Also select either 3.3V or 5V as your system voltage (Vport), which is used by many other features on the board.

Power (using USB based connection)

5V:	4.4V to 5.5V (depends on the PC USB voltage provided) – 200mA available for UUT
3.3V:	Regulated – 300mA available for UUT

Power (using optional external DC power connection)

Vjack:	6V to 15V DC input from external supply (wall-wart)
5V:	Regulated 5.0V at 800mA
3.3V:	Regulated 3.3V at 800mA

Workspace Power (powers all debug devices on the work surface)

Vport	Selectable from 5V or 3.3V supplies

USBee AX Test Pod (2)

Oscilloscope, Logic Analyzer, Signal Generator, Frequency Counter and more. Refer to the USBee AX Users Manual for details. Also includes Logic Probe LEDs to instantly see the state of logic levels.

Physical: Located on the top work surface

Test Functions: 24Msps Mixed Signal Logic Analyzer / Oscilloscope (1Ax8D), Signal Generator

Connections: 0.1" spaced 0.025" pin male header connects 9" test lead set

Logic Probe: 8 channel logic probe (runs independent of the USBee AX)

Please refer to the USBee AX Test Pod User's Manual for complete feature descriptions

Debug Center (3)

Reconfigurable ports. Click on the schematic in the USBee Suite software to define what these ports become. Need an inverter? Done. Need an Op Amp? Done! See the details to the left of some of the physical devices available.

Physical: Locate on the top work surface

Configurations: Detailed configuration schematics and descriptions are in the Appendix A

Reconfig Time: 10 seconds

Power: 0V to Vport operation

Connections: 2 8-bit ports that are reconfigurable

Sample Functions: Op Amp, PGA, Logic, Level Shifter, Flip Flops, LEDs, Counters, Comparitors, etc.

Internal Hardware: Based on the Cypress Semiconductor PSoC3

All features of the Debug Center are implemented in the PSoC3. All of the specifications for the components follow directly from the PSoC3 Datasheet. For more details, please visit www.cypress.com/psoc3

Voltmeters (4)

Measure up to 4 channels of DC voltage from GND to VPort. Great for battery monitoring, reference voltages and logic levels.

Channels: 4

Voltage Range: 0V to VPort

Resolution: 8-bits (Vport / 256)

Accuracy: +/- 3% of Vport

Update Rate: 250msec

Input: 500k || 20pf

Edge Detectors (5)

Detects if the signals ever cross the Vport/2 voltage threshold. Need to run a test over the long haul? Make it toggle a pin in the event of an error. These LEDS will then light if this event ever happens

Channels: 4

Voltage Range: 0 to Vport

Logic Threshold: Vport / 2

Threshold Accuracy: +/- 10% of Vport

Minimum Pulse Width: 5ns

Input: 500k || 20pf

Async Port (6)

This port shows up as a COM port on the PC. Simply choose your baud rate and your device can send data to Hyperterminal, putty, etc., as well as be controlled by the PC. The COM port number is displayed in the USBee Suite Protolyzer Control Panel.

Channels: 2 (1 to the PC, 1 from the PC)

Voltage Range: 0 to Vport

Logic Threshold: Vport / 2

Threshold Accuracy: +/- 10% of Vport

Baud Rate: 110 to 3,000,000 baud

Protocol: No parity, 8 data bits, 1 stop bit

Input: 500k || 20pf

PC interface: COM port appears on PC

Function Generator (7)

Create Sine, Triangle and Square waves at any frequency between 0 Hz and 6MHz. Uses a DDS with 24MHz clock to derive finely tuned frequencies. Sine and Triangle waves are GND to 3.3V. Square waves are GND to Vport.

Channels: 2 (1 sine/triangle, 1 square)

Voltage Out: Sine / Triangle: 0V to 3.3V, Square Wave: 0V to Vport

Frequency: 0 Hz to 6MHz

Resolution: 1% of set frequency (5Hz at 500Hz, 30kHz at 3MHz)

Ripple: +/- 50mV

Freq Accuracy: +/- 300ppm

Square Wave Duty Cycle: 40% to 60%

Voltage Out (8)

Generate variable DC voltage out using either the on board up and down buttons or the USBee Suite PC interface.

Channels: 1

Voltage Out: 0V to Vport

Resolution: Vport / 256

Buttons: 2 (Up and Down in Resolution steps)

Ripple: +/- 50mV

Voltage Accuracy: +/- 50mV

Drive Current: 25mA

Dip Switches (9)

Channels: 8

Common: Common side connect to 0V or Vport through switch

Setting: On or Off via micro slide switch

Current: up to 100mA

LEDs (10)

Channels: 8

Logic: 0V is OFF, Vport is ON

Threshold: 1.4V

Input Current: < 1mA

Variable Potentiometers (11)

Number: 2 (1 - 10K, 1 – 20K)

Type: Thumbwheel

Range: 1K to 10K, 2K to 20K

Current: < 10mA

Push Buttons (12)

Number: 4

State: Normally Open

Current: 100mA

Contacts: 2 – shorted together when button pressed

Slide Switches (13)

Number: 4

Type: SPST, Make before Break

Current: 100mA

Contacts: 3 – 1 and 2 shorted or 2 and 3 shorted

USBee Suite Control (14)

Lets you capture traces, pan and zoom without leaving the Protolyzer. Also launch any file/url/app with a single press of the Macro key.

Buttons: 6 (Pan +, Pan -, Zoom +, Zoom -, Capture, Macro)

Power Bar (15)

Power headers are adjacent to the work area for easy connection. Choose from GND, 3.3V, 5V, VBus or Vjack

Solderless Breadboard (16)

Great place to mount your design. Add pins to your design Vcc and GND and plug them into this board. Holds your board in place and lets you route power and ground easily.

Spacing: 0.1" spaced holes

Total Connections: 128 connections with 5 holes each (640 holes)

Power Strip: 4 bussed power lines

Wires: 150 wires with lengths from 0.1" to 5"

Dimensions: 2" x 6.5"

Physical

Size: 6.5”W x 8.5”L x 3”H (DX Protolyzer)

6.5”W x 8.5”L x 1”H (AX Protolyzer)

Weight: 1.5 pounds (DX Protolyzer)

0.5 pounds (AX Protolyzer)

Case: DX Only - Black slanted plastic. Workspace on top. USBee DX connections out the back

Operating Temperature: 10C to 50C

Storage Temperature: 0C to 70C

External Connections

To PC: DX Protolyzer – One 6 foot USB 2.0 High Speed (cable provided) provides power

AX Protolyzer – Two 6 foot USB 2.0 High Speed (cables provided) for Power/USBee AX and Debug Center. The DX Protolyzer has an internal Hub that makes these connections.

External Power: (Optional) DC power supply connection for higher current and voltage needs

DX Oscilloscope: 2 standard 40Mhz oscilloscope probes – x1 and x10 selectable

DX Digital Channels: Test Leads are 9” long with 0.025” square sockets on the ends.

AX Oscilloscope: 1 standard 40Mhz oscilloscope probe – x1 and x10 selectable

AX Digital Channels: Test Leads are 9” long with 0.025” square sockets on the ends.

USBee DX Test Pod (back of unit)

Physical: Located internal to the Protolyzer case. Connections out the back of unit

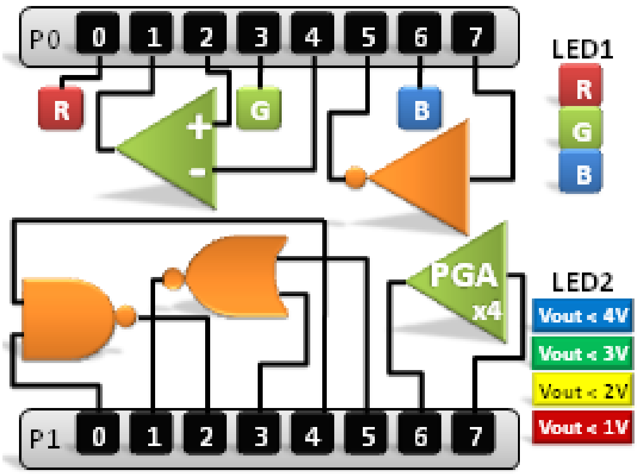
Connections: 2x10 set of 9” test leads, 2 standard 40Mhz BNC oscilloscope probes and USB mini-B

Test Functions: 24Msps Mixed Signal Logic Analyzer / Oscilloscope (2Ax16D), Signal Generator

Please refer to the USBee DX Test Pod User’s Manual for complete feature descriptions.

Appendix A

Debug Center Configurations



Analog and Digital Configuration 00001

Overview

This configuration contains a mixture of the following analog and digital functions:

- Op Amp (GND to Vport supplies)
- 4X Gain Amplifier (GND to Vport Supplies)
- 2 input NAND logic gate
- 2 input NOR logic gate
- Inverter (NOT) logic gate
- Red, Green and Blue digital input control lines for Tri-color LED1
- LED2 color based on Vout voltage level

Op Amp Details

The Operational Amplifier (Opamp) component provides a basic Opamp configuration. The Opamp should be used anytime a voltage output needs to drive a load of less than 10KOhms. The Opamp may be used as a generic Opamp with external components. The Op Amp uses the GND and Vport as its supply voltages.

Input/Output Connections

This section describes the various input and output connections for the Opamp.

Non-Inverting (+) - This is the standard Opamp non-inverting input.
Inverting (-) - This is the standard Opamp inverting input.
Voutput - This is the standard Opamp output signal. It is capable of driving 25mA.

Programmable Gain Amplifier (PGA) Details

The PGA component implements an Opamp-based non-inverting amplifier with defined gain. This amplifier has high input impedance and wide bandwidth. The PGA is used anytime a signal does not have sufficient amplitude. A PGA may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude. The PGA uses the GND and Vport as its supply voltages.

Input/Output Connections

This section describes the various input and output connections for the PGA.

- **Vin -** the voltage input.
- **Vref -** the input terminal for a reference signal. If there is no Vref signal, it is internally connected to GND.
- **Voutput -** the output voltage signal terminal. Voutput is a function of (Vin - Vref) times the specified Gain. It is capable of driving 25mA.
  *Voutput = Vref + (Vin - Vref) * Gain*

Logic Gates (AND, OR, NAND, NOR, XOR, XNOR, Inverter - NOT) Details

Logic gates provide basic boolean operations. The output of a logic gate is a boolean combinatorial function of the inputs. There are seven basic logic gates: AND, OR, Inverter (NOT), NAND, NOR, XNOR, and XOR. The logic gates use the GND and Vport as supply voltages. The logic levels are set at Vih = 2.0V, Vil = 0.8V, Voh = Vport, Vol = GND.

Use logic gates when you want to perform basic logical operations. You can perform more complex operations with various combinations of the basic logic gates.

Functional Description

This section describes each of the logic gates separately. The gate logic descriptions use the following convention to describe logic levels:

True = 1 = high logic level
False = 0 = low logic level

AND Gate

The AND gate performs logical multiplication in the same way as the logical AND operator. It has two or more inputs and one output. As shown in the following truth table, the output is true when all inputs are true. Otherwise, the output is "false."

Table 1: AND Truth Table

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

The OR gate performs logical addition in the same way as the logical inclusive OR operator. It has two or more inputs and one output. As shown in the following truth table, the output is true if the inputs are true. If all inputs are false then the output is false.

Table 2: OR Truth Table

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Inverter (NOT) Gate

The Inverter, also called a NOT gate, performs the basic logic function called inversion. In other words, this gate changes one logic level (true/false) to the opposite logic level. The NOT gate has only one input and one output. As shown in the following truth table, the output is false when the input is true and vice-versa.

Table 3: Inverter (NOT) Truth Table

Input	Output
1	0
0	1

XOR Gate

The XOR (exclusive-OR) gate is useful as a parity generator. It has two or more inputs and one output. As shown in the following truth table, the output is true when there are an odd number of true inputs. Otherwise, the output is false.

Table 6: XOR Truth Table

Input 1	Input 2	Input 3	Output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

XNOR Gate

The XNOR (exclusive-NOR) gate is useful as a parity generator. It has two or more inputs and one output. As shown in the following truth table, the output is false when there are an odd number of true inputs. Otherwise, the output is true.

Table 7: XNOR Truth Table

Input 1	Input 2	Input 3	Output
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

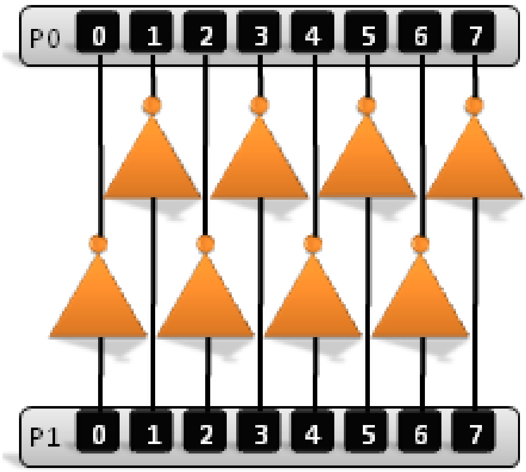
Tri-Color LED Control

The R, G and B digital input signals are sampled to drive the Tri-Color LED. The following table shows the colors generated by various R, G and B settings:

R (Red Input)	G (Green Input)	B (Blue Input)	LED Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.



Digital Configuration 00002

Overview

This configuration contains 8 logic inverters (NOT)

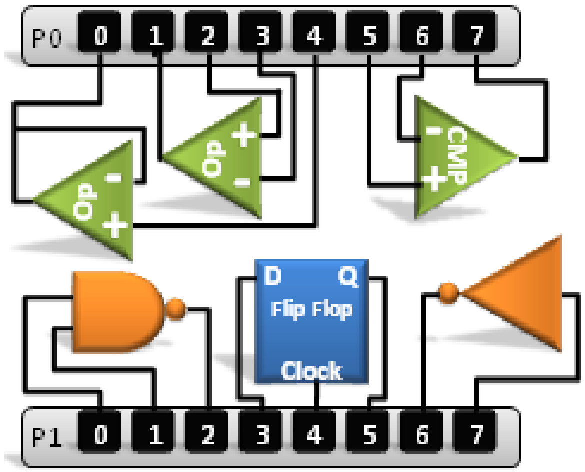
Logic Gates (AND, OR, NAND, NOR, XOR, XNOR, Inverter - NOT) Details

Logic gates provide basic boolean operations. The output of a logic gate is a boolean combinatorial function of the inputs. There are seven basic logic gates: AND, OR, Inverter (NOT), NAND, NOR, XNOR, and XOR. The logic gates use the GND and Vport as supply voltages. The logic levels are set at Vih = 2.0V, Vil = 0.8V, Voh = Vport, Vol = GND.

Use logic gates when you want to perform basic logical operations. You can perform more complex operations with various combinations of the basic logic gates.

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.



Analog and Digital Configuration 00003

Overview

This configuration contains a mixture of the following analog and digital functions:

- Op Amp (GND to Vport supplies)
- Op Amp in voltage follower configuration (GND to Vport Supplies)
- Voltage Comparator
- D Flip Flop
- 2 input NAND logic gate
- Inverter (NOT) logic gate

Comparator Details

The Comparator component provides a hardware solution to compare two analog input voltages. The Comparator can provide a fast comparison between two voltages as compared to using an ADC. A common configuration is to create an adjustable comparator by connecting a voltage DAC to the negative input terminal. This comparator includes 10mV of hysteresis.

Input/Output Connections

This section describes the various input and output connections for the Comparator.

Positive Input - This input is usually connected to the voltage that is being compared.

Negative Input - This input is usually connected to the reference voltage.

Comparator Out - The digital output (0 to Vport) of the comparison. This output goes high when the positive input voltage is greater than the negative input voltage.

D Flip Flop Details

The D Flip Flop stores a digital value and should be used to implement sequential logic. This component operates from GND to Vport.

Input/Output Connections

This section describes the various input and output connections for the D Flip Flop.

D Input - This input determines the next value of the output. The output does not change until the next rising edge of the clock.
Clock Input - The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.
Q Output - The stored value of the D Flip Flop.

Op Amp Details

The Operational Amplifier (Opamp) component provides a basic Opamp configuration. The Opamp should be used anytime a voltage output needs to drive a load of less than 10KOhms. The Opamp may be used as a generic Opamp with external components. The Op Amp uses the GND and Vport as its supply voltages.

Input/Output Connections

This section describes the various input and output connections for the Opamp.

Non-Inverting (+) - This is the standard Opamp non-inverting input.
Inverting (-) - This is the standard Opamp inverting input.
Voutput - This is the standard Opamp output signal. It is capable of driving 25mA.

Programmable Gain Amplifier (PGA) Details

The PGA component implements an Opamp-based non-inverting amplifier with defined gain. This amplifier has high input impedance and wide bandwidth. The PGA is used anytime a signal does not have sufficient amplitude. A PGA may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude. The PGA uses the GND and Vport as its supply voltages.

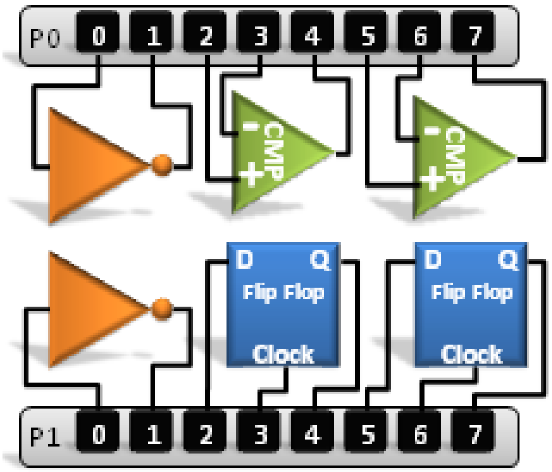
Input/Output Connections

This section describes the various input and output connections for the PGA.

- **Vin -** the voltage input.
- **Vref -** the input terminal for a reference signal. If there is no Vref signal, it is internally connected to GND.
- **Voutput -** the output voltage signal terminal. Voutput is a function of (Vin - Vref) times the specified Gain. It is capable of driving 25mA.
  *Voutput = Vref + (Vin - Vref) * Gain*

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.



Analog and Digital Configuration 00004

Overview

This configuration contains a mixture of the following analog and digital functions:

- 2 D Flip Flops
- 2 Inverter (NOT) logic gates
- 2 Voltage Comparators

Comparator Details

The Comparator component provides a hardware solution to compare two analog input voltages. The Comparator can provide a fast comparison between two voltages as compared to using an ADC. A common configuration is to create an adjustable comparator by connecting a voltage DAC to the negative input terminal. This comparator includes 10mV of hysteresis.

Input/Output Connections

This section describes the various input and output connections for the Comparator.

Positive Input - This input is usually connected to the voltage that is being compared.
Negative Input - This input is usually connected to the reference voltage.
Comparator Out - The digital output (0 to Vport) of the comparison. This output goes high when the positive input voltage is greater than the negative input voltage.

D Flip Flop Details

The D Flip Flop stores a digital value and should be used to implement sequential logic. This component operates from GND to Vport.

Input/Output Connections

This section describes the various input and output connections for the D Flip Flop.

D Input - This input determines the next value of the output. The output does not change until the next rising edge of the clock.
Clock Input - The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.
Q Output - The stored value of the D Flip Flop.

Op Amp Details

The Operational Amplifier (Opamp) component provides a basic Opamp configuration.   The Opamp should be used anytime a voltage output needs to drive a load of less than 10KOhms. The Opamp may be used as a generic Opamp with external components. The Op Amp uses the GND and Vport as its supply voltages.

Input/Output Connections

This section describes the various input and output connections for the Opamp.

Non-Inverting (+) - This is the standard Opamp non-inverting input.
Inverting (-) - This is the standard Opamp inverting input.
Voutput - This is the standard Opamp output signal. It is capable of driving 25mA.

Programmable Gain Amplifier (PGA) Details

The PGA component implements an Opamp-based non-inverting amplifier with defined gain. This amplifier has high input impedance and wide bandwidth. The PGA is used anytime a signal does not have sufficient amplitude. A PGA may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude. The PGA uses the GND and Vport as its supply voltages.

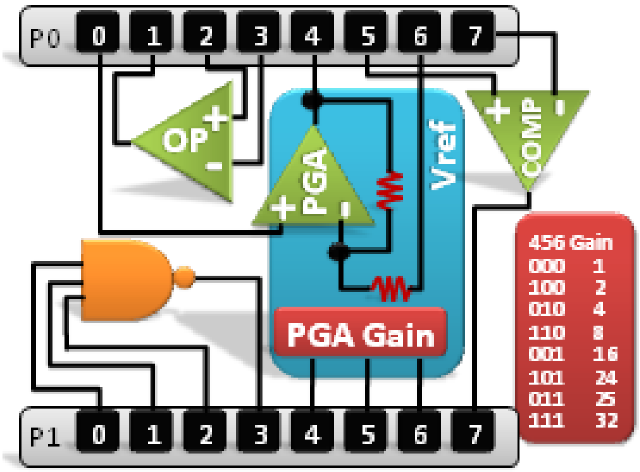
Input/Output Connections

This section describes the various input and output connections for the PGA.

- **Vin -** the voltage input.
- **Vref -** the input terminal for a reference signal. If there is no Vref signal, it is internally connected to GND.
- **Voutput -** the output voltage signal terminal. Voutput is a function of (Vin - Vref) times the specified Gain.   It is capable of driving 25mA.
  *Voutput = Vref + (Vin - Vref) * Gain*

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.



Analog and Digital Configuration 00005

Overview

This configuration contains a mixture of the following analog and digital functions:

- Op Amp (GND to Vport supplies)
- Programmable Gain Amplifier (GND to Vport Supplies)
- 1 input NAND logic gate
- Voltage Comparator

Op Amp Details

The Operational Amplifier (Opamp) component provides a basic Opamp configuration. The Opamp should be used anytime a voltage output needs to drive a load of less than 10KOhms. The Opamp may be used as a generic Opamp with external components. The Op Amp uses the GND and Vport as its supply voltages.

Input/Output Connections

This section describes the various input and output connections for the Opamp.

Non-Inverting (+) - This is the standard Opamp non-inverting input.
Inverting (-) - This is the standard Opamp inverting input.
Voutput - This is the standard Opamp output signal. It is capable of driving 25mA.

Programmable Gain Amplifier (PGA) Details

The PGA component implements an Opamp-based non-inverting amplifier with programmable gain. This amplifier has high input impedance and wide bandwidth. The PGA is used anytime a signal does not have sufficient amplitude. A PGA may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude. The PGA uses the GND and Vport as its supply voltages. The Gain chosen is selected by the 3 digital inputs. The Vref signal is used to provide an offset to the output voltage. The *Voutput = Vref + (Vin - Vref) * Gain.*

The Gain can be set to the following values: 1, 2, 4, 8, 16, 24, 25, and 32

Input/Output Connections

This section describes the various input and output connections for the PGA.

- **Vin -** the voltage input.
- **Vref -** the input terminal for a reference signal. If there is no Vref signal, it is internally connected to GND.
- **Voutput -** the output voltage signal terminal. Voutput is a function of (Vin - Vref) times the specified Gain. It is capable of driving 25mA.
  *Voutput = Vref + (Vin - Vref) * Gain*

Comparator Details

The Comparator component provides a hardware solution to compare two analog input voltages. The Comparator can provide a fast comparison between two voltages as compared to using an ADC. A common configuration is to create an adjustable comparator by connecting a voltage DAC to the negative input terminal. This comparator includes 10mV of hysteresis.

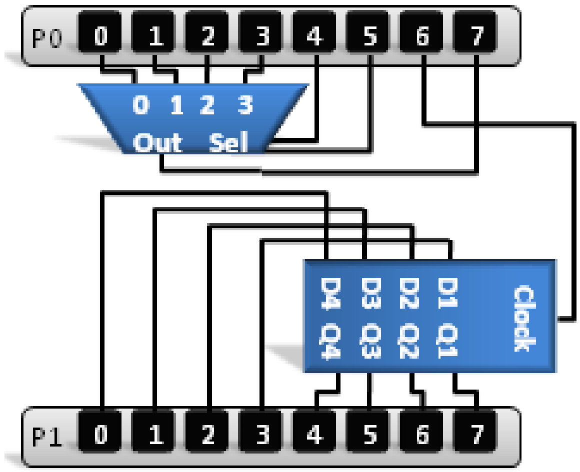
Input/Output Connections

This section describes the various input and output connections for the Comparator.

Positive Input - This input is usually connected to the voltage that is being compared.
Negative Input - This input is usually connected to the reference voltage.
Comparator Out - The digital output (0 to Vport) of the comparison. This output goes high when the positive input voltage is greater than the negative input voltage.

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.



Digital Configuration 00006

Overview

This configuration contains a mixture of the following analog and digital functions:

- 4 Channel D Flip Flop
- 4 to 1 Digital Multiplexer

D Flip Flop Details

The D Flip Flop stores a digital value and should be used to implement sequential logic. This component operates from GND to Vport.

Input/Output Connections

This section describes the various input and output connections for the D Flip Flop.

D Inputs (D1 to D4) - This input determines the next value of the output. The output does not change until the next rising edge of the clock.

Clock Input - The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.

Q Outputs (Q1 to Q4) - The stored value of the D Flip Flop for that channel.

Digital Multiplexer Details

The Digital Multiplexer is a device that performs multiplexing: it selects one of many digital input signals and forwards the selected input into a single output line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. This component operates from GND to Vport.

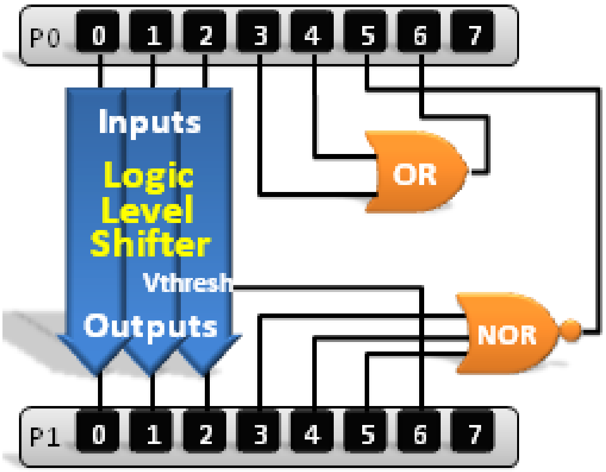
Input/Output Connections

This section describes the various input and output connections for the D Flip Flop.

Inputs - These are the inputs to choose from.

Output – This is the selected signal determined by the Select Lines.

Select Line(s) – These are the control lines that determine which of the Input signals will get routed to the Output signal.



Digital Configuration 00007

Overview

This configuration contains a mixture of the following analog and digital functions:

- 3 Channel Digital Voltage Level Shifter
- 2 Input OR Logic Gate
- 3 Input NOR Logic Gate

Digital Voltage Level Shifter Details

This feature is invaluable for converting low voltage logic levels (< 1.8V logic) to the logic levels required by the USBee Logic Analyzers. The Digital Voltage Level Shifter takes a digital logic signal with a lower threshold and converts it to GND-Vport logic levels. The input threshold is set using the VThresh input signal. There is about 10mV of input hysteresis and the VThresh can be set anywhere from GND to VPort. You can use the Vout signal to set the voltage level you need for the logic family you are using. For example, for 1.2V logic you can set the VThresh to 0.6V by inputting this voltage into the VThresh pin.

Input/Output Connections

This section describes the various input and output connections for the D Flip Flop.

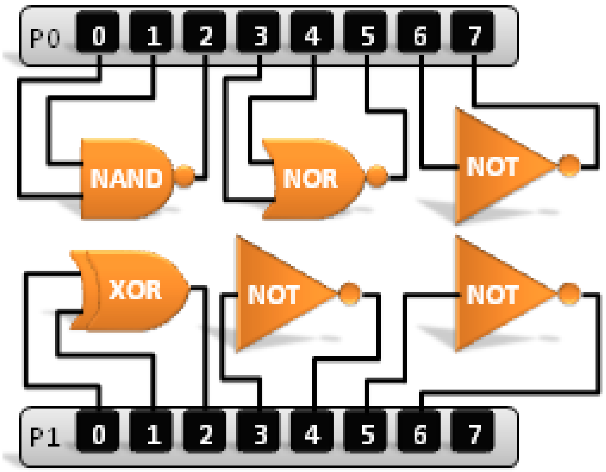
Inputs – The input logic signal.

VThresh Input – An analog voltage that defines the threshold. If the Input signal is below this voltage a logic 0 (GND) is output on the Output signal. If the Input signal is above this voltage a logic 1 (Vport) is output on the Output signal.

Outputs - The resulting output signal after level shifting.

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.



Digital Configuration 00008

Overview

This configuration contains a mixture of the following analog and digital functions:

- 2 input NAND logic gate
- 2 input NOR logic gate
- 2 input XOR logic gate
- 3 Inverter (NOT) logic gates

Additional Specifications

The USBee Protolyzer Debug Center features are implemented using the Cypress Semiconductor PSoC3 IC. For this reason, the specifications for the chosen components are derived directly from the PSoC3 specifications. For more information, please visit www.cypress.com and search for PSoC3.